Pramod Udupa

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Objective

To pursue excellence in the field of digital ASIC/FPGA design and contribute to it. VLSI Systems Engineer with more 2 years of experience in ASIC/FPGA design flows/tools.

Current Position

Jan.2011–Jan.2014 **Ph.D**, *INRIA Rennes*, Lannion.
Worked on low-complexity algorithms and high-speed parallel architectures for 100 Gbps Coherent Optical OFDM Systems, [Expected Date of Completion: March 2014]

Academic Qualifications

2006–2008 **Master of Engineering**, *BITS, Pilani*, Pilani, *CGPA - 9.2/10*.
Specialized in Mircoelectronics & VLSI

2002–2006 **Bachelor of Engineering**, *M.S.R.I.T*, Bangalore, *Percentage - 81%*.
Electronics & Communication Engineering

Professional Experience

Aug.2008–Dec.2010 **Research Assistant**, *I.I.Sc*, Bangalore.
Worked on Acceleration of Numerical Linear Algebra Kernels on FPGA using Bluespec System Verilog (BSV)

Jan.2008–Jun.2008 **Internship**, *NXP Semiconductors*, Bangalore.
Worked on Power planning strategy for sizing power grid structure for a complex SoC

Technical skills

Design Entry	Verilog, VHDL, CatapultC HLS, Vivado HLS, C/C++, Bluespec System Verilog (BSV)
FPGA Design Tools	Xilinx ISE, Altera Quartus, SOPC Builder
ASIC Design Tools	Modelsim, Design Compiler, PrimeTime, SoC Encounter
Productivity Tools	Matlab, MS Office, LaTeX, Tcl
Operating Systems	Windows, Mac OS X, Linux
Communication Standards	802.11a WiFi

[1]French National Institute for Research in Computer Science and Control
[2]Institute for Research in Computer Science and Random Systems

Major Subjects	Digital VLSI, Computer Architecture, OFDM Systems, Parallel Architectures, DSP Algorithms and Architectures, Fixed-Point Systems

Projects Done

OFDM Transceiver	Design and implementation of end-to-end parallel OFDM transceiver system using CatapultC tool. Fixed-point Optimization of the architecture is done and performance of the system is characterized by using data from experiment. Verilog generated is targeted to Xilinx FPGA and ASIC design flow.
CO-OFDM Algorithms	Developed algorithms for decoding data in Coherent Optical OFDM system and validated using experimental data in Matlab. A novel synchronization algorithm was developed.
Power grid Sizing	Allocation and sizing of resources for power grid design in SoC. The sizing was tested on two complex SoC's and analysis of IR Drop done to validate the sizing.
ALU of DSP	Design of ALU of a DSP using Verilog HDL and implemented using ASIC design flow.
DAC	Design of 10-bit Voltage mode DAC.
TLP	Study of Thread Level Parallelism in Multi-Core Architectures.

Ph.D thesis

title	*Sampling, synchronization, digital processing and FPGA implementation of 100Gbps CO-OFDM systems*
supervisors	Olivier SENTIEYS and Laurent BRAMERIE
description	Thesis is done in CAIRN team of INRIA[1]/IRISA[2]. The thesis focuses on developing parallel low complexity algorithms and architectures for a high speed 100Gbps CO-OFDM system implemented on a FPGA board. Contributions include low-complexity timing synchronization and parallel architectures for timing synchronization,FFT/IFFT and scalable parallel CO-OFDM transceiver architecture for very high speed signal processing. The development of communication IPs is done using CatapultC high level synthesis (HLS) tools from which HDL is generated for synthesis.

Master thesis

title	*Power Planning Strategy to implement complete Power Grid Structure for a complex SoC and its validation*
supervisors	Viswanathan N and Anu Gupta
description	In this thesis, a power planning strategy for sizing the metal widths for power supply was designed. The metal widths are calculated based on constraints like maximum IR-drop, maximum metal width available at a particular layer. The methodology was tested on two real large SoC designs for its validation.

Publications

P. Udupa, O. Sentieys and P. Scalart. ***A Novel Hierarchical Low Complexity Synchronization Method for OFDM Systems***. in IEEE 77th Vehicular Technology Conference Spring, 2013.

P. Udupa, O. Sentieys and P. Scalart. ***A Block-Parallel Architecture for Initial and Fine Synchronization in OFDM Systems***. in IEEE International Conference on Communications, 2013.

P. Biswas, **P. Udupa** et al. ***Accelerating Numerical Linear Algebra Kernels on a Scalable Run Time Reconfigurable Platform***. in IEEE Computer Society Annual Symposium, 2010.

A. Rao and **P. Udupa**. ***A Hardware Accelerated System for Deep Packet Inspection***. in 8th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), 2010.

Academic Honours

GATE	Scored 488th rank in GATE 2008
Scholarship	My entire M.E program in BITS,Pilani was funded by NXP Semiconductors scholarship, which is given to selected few M.E students in IITs/BITS
IIRC	Participated upto the penultimate round in Intel India Research Challenge 2006-07

Languages

English	**Professional Proficiency**
French	**Limited Working Proficiency**
Hindi	**Working Proficiency**
Kannada	**Native Language**

References

Available upon request

Personal Information

Nationality	Indian
Date of Birth	19/06/1984