

## Master de Recherche – Master of Research

Title: Energy Optimization of Network-On-Chip

Keywords and skills: Network-on-chip, power consumption, optimization, design

Laboratory: IRISA/INRIA –CAIRN project-team (Lannion)

<http://www.irisa.fr/activity/research/cairn> <http://www.irisa.fr/cairn/jobs>

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### Context:

The current trend of integration and performance is based on the integration of many processors (dedicated or general) on a single chip, so called "Multi-Processor-on-Chip (MPSoC). These embedded systems must interact with their environment to adapt to the outside world or will face changes in user demand. Flexibility is become a major property of such systems. The need for flexibility and performance has led us to propose a dynamically reconfigurable MPSoC. The principle comes from the ability to change a system's processors online, i.e. while the others continue their execution.

This massive parallelism imposes new constraints on the communication media. The traditional communications bus will not allow scaling and many works have started on the definition of integrated network on chip (NoC for Network on Chip) that allows first to support flexible architectures and efficient communication and secondly to support a growing number of computing processors. In this sense we have designed an efficient NoC for dynamically reconfigurable MPSoC.

In the same time the power consumption constraint is becoming problematic. Power consumption reduction techniques are being applied everywhere in computer systems and the interconnection network is not an exception, as its contribution is not negligible. As our network is based on a tree structure, it can be optimized in power consumption by using several approaches.

### Objectives:

The objective of this course is to study, to select and validate low-power strategies to be integrated in the DRAFT network. As a first step we will study several approaches (clock gating, coding, DVFS) that can be integrated in the NoC. A fast evaluation of the effectiveness of the different approaches will be conducted by using evaluation environment.

In a second step, the selected strategies will be implemented on a Virtex5 platform, and power savings will be evaluated in-situ against a non-optimized system. All the proposed solutions must support the required performance of nowadays applications, and need to not reduce the flexibility of the MPSoC ( i.e. support dynamic reconfiguration paradigm).

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