Hardware implementation of the arithmetic of fields of characteristic 2 and 3

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Introduction

- Curve-based cryptography relies on finite fields
  - Among them: small characteristic fields (2 and 3)
    * Example: pairings on supersingular elliptic curves

- Need for hardware implementations
  - Embedded systems (RFID, smart card, sensors, ...)
  - High-performance cryptographic coprocessor (bank servers, ...)
    * No native support in CPUs (Partial support in Intel AVX instruction set)
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  - great prototyping platform
  - flexibility when increasing security is needed
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- Join work with:
  - Jean-Luc Beuchat, LCIS, University of Tsukuba, Japan.
  - Jérémie Detrey, CARAMEL project-team, INRIA Nancy Grand-Est, France.
FPGA architecture

▶ FPGAs are composed of:

- programmable logic cells
- a configurable routing matrix
- input/output cells
- embedded memory blocks
- small embedded multipliers
- etc.

Inside a logic cell:

- connections to the routing matrix
- programmable lookup-tables
  - 4 inputs, 1 output
  - 6 inputs, 1 output
  - 6 inputs, 2 outputs
- optional registers
  - free pipelining
- more logic for fast carry-propagation
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![FPGA architecture diagram](image-url)
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Outline of the talk

- Small characteristic finite fields
- Multiplication algorithms and hardware implementation
- A finite field coprocessor
- Finite fields of composite extension degree
Representation of the elements

- Small characteristic: $p = 2$ or $3$

- Polynomial basis:
  - $\mathbb{F}_{p^m} = \mathbb{F}_p[x]/(f(x))$
  - $f(x)$ irreducible polynomial of degree $m$
  - $\mathbb{F}_{p^m}$ represented by $\mathbb{F}_p[x]^{(m-1)}$
  - Reduction modulo $f(x)$ possibly required

- Operations in the field
  - Addition
  - Frobenius automorphism: $(\cdot)^p$
  - Multiplication
  - Inversion
    - Itoh & Tsujii algorithm (Fermat's little theorem)
    - or Extended Euclidean algorithm
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Hardware implementation of addition

\[ a \oplus b \]

Representation of coefficient

- \( F_2 \): two values → one wire, addition is the XOR boolean operator
- \( F_3 \): three values → borrow-save representation on two wires

Opposite of a coefficient: swap the two wires
Hardware implementation of addition

\[ a_{m-1}b_{m-1} a_{m-2}b_{m-2} \]

\[ a_1 b_1 a_0 b_0 \]

\[ \text{Add coefficient-wise} \]
Hardware implementation of addition

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Computation of the Frobenius automorphism

\[ a^p \equiv (a_{m-1}x^{m-1} + \cdots + a_1x + a_0)^p \pmod{f(x)} \]

- Raising to the \( p \)-th power

- Since \( \binom{p}{i} \equiv 0 \pmod{p} \) when \( i \neq 0 \), non-linear terms disappear

- Need reduction
  - reduce each \( x^p \cdot i \) linear combination of the coefficients
    - \( f \) with low Hamming weight
    - tri- or pentanomials
    - each coefficient of the results is the sum of few coefficients

- Hardware implementation
  - Selection of coefficient is free (just wiring!)
  - Same cost as for a few additions
  - Depending on LUTs' size, one LUT per coefficient might be enough
Computation of the Frobenius automorphism

\[ a^p \equiv a_{m-1} x^{p(m-1)} + \cdots + a_1 x^p + a_0 \pmod{f(x)} \]

- Raising to the \( p \)-th power
- Linear operation
  - Since \( \binom{p}{i} \equiv 0 \pmod{p} \) when \( i \neq 0 \), non-linear terms disappear
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\[ a^p \equiv (a_{\sigma_{m-1}(0)} + a_{\sigma_{m-1}(1)} + \cdots) x^{p-1} + \cdots \pmod{f(x)} \]

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Fermat’s little theorem

\[ a^{-1} \equiv a^{p^m-2} \pmod{f} \]
Itoh & Tsujii algorithm

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- Computation of \( a^{p^m-2} \) only needs:
  - \( (m - 1) \) Frobenius automorphism applications
  - few multiplications
  - an inversion in \( \mathbb{F}_p \)
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No need for supplementary hardware
Itoh & Tsujii algorithm

► Fermat’s little theorem

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► Computation of \( a^{p^m - 2} \) only needs:
  
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Naive algorithm

- Schoolbook algorithm
  - express each partial product
  - add them
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- **Schoolbook algorithm**
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  - add them

- Reduction modulo $f$ needed
**Naive algorithm**

- **Schoolbook algorithm**
  - express each partial product
  - add them

- **Reduction modulo $f$ needed**

- **Reduce** each partial product sequentially

$$a \cdot b \equiv a \cdot b_0 + a \cdot b_1 + \cdots + a \cdot b_{m-2} + a \cdot b_{m-1} \cdot x \pmod{f}$$

$$a \cdot b \equiv (a \cdot b_0 + a \cdot b_1 + \cdots + a \cdot b_{m-1}) \cdot x \pmod{f}$$
Naive algorithm

Schoolbook algorithm
- express each partial product
- add them

Reduction modulo $f$ needed

Reduce and accumulate each partial product sequentially

$$a \cdot b \pmod{f}$$
Parallel-serial multiplier

- Operand $a$ is treated in parallel
- Operand $b$ is treated $D$ coefficients per cycle
- Need $\lceil m/D \rceil$ cycles to complete the product
Karatsuba algorithm

\[ A \cdot B \]

\[ A = AHBHX \]
\[ B = BLALAH \]
\[ A \cdot B = (A + A') (B + B') - AB - A'B' \]
Karatsuba algorithm

\[ A_H B_H X^{2n} + (A_H B_L + A_L B_H)X^n + A_L B_L \]
Karatsuba algorithm

\[ A_H B_H X^{2n} + (A_H B_L + A_L B_H) X^n + A_L B_L \]

\[ ab' + a'b = (a + a')(b + b') - ab - a'b' \]

\[ A_H B_H X^{2n} + ((A_H + A_L)(B_H + B_L) - A_H B_H - A_L B_L) X^n + A_L B_L \]
Karatsuba algorithm

\[ A_H \cdot B_H + (A_H \cdot B_L + A_L \cdot B_H) \cdot X^n + A_L \cdot B_L \]

\[ a \cdot b + a' \cdot b' = (a + a')(b + b') - ab - a'b' \]
Karatsuba algorithm

\[ A \cdot B = (A_H \cdot B_H + A_L \cdot B_L) \cdot X^n + (A_H \cdot B_L + A_L \cdot B_H) \cdot X \]

3-way Karatsuba

- split operands in three parts
- only 6 subproducts needed
Karatsuba algorithm

\[ A_H \cdot A_L \quad \underline{+} \quad B_H \cdot B_L \]

\[ + \quad - \quad - \quad + \]

\[ A \cdot B \]

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Odd-even split for Karatsuba multiplication

\[ A \cdot B \]
Odd-even split for Karatsuba multiplication

\[(A_O B_O X^2 + A_E B_E) + X(A_O B_E + A_E B_O)\]
Odd-even split for Karatsuba multiplication

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\[ \begin{align*}
A_O \cdot B & \quad \text{...} \\
A_E & \\
B_O \cdot B_E & \quad \text{...}
\end{align*} \]
Fully parallel pipelined Karatsuba multiplier

- **Karatsuba-like algorithm:**
  - split the operands
  - compute the subproducts
  - recompose the result

- **Fully parallel** evaluation of the subproducts

```
a \times b
\sim \frac{a + c}{2} \times \frac{b + d}{2} + \frac{a - c}{2} \times \frac{b - d}{2}
```

```
\text{Splitter} \rightarrow \text{Multipliers} \rightarrow \text{Recomposer}
```

```
\text{A} \times \frac{a + c}{2} \times \frac{b + d}{2} \rightarrow \text{Multipliers} \rightarrow \text{A} \times \frac{a - c}{2} \times \frac{b - d}{2} \rightarrow \text{Recomposer}
```

```
\text{A} \cdot B
```

N. Estibals — Hardware implementation of the arithmetic of fields of characteristic 2 and 3
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- **Recursive** scheme
  - eventually use different multiplication algorithms
  - end with the **quadratic** paper-and-pencil algorithm

![Diagram of Karatsuba multiplier](attachment:karatsuba_diagram.png)
Fully parallel pipelined Karatsuba multiplier

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Pipelined
- with the help of optional registers
- cut the critical path
- increase the frequency
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- **Final reduction** modulo $f$
An example of multipliers over $\mathbb{F}_{3}^{239}$

$\mathbb{F}_{3}^{239} = \mathbb{F}_3[X]/(X^{239} - X^5 + 1) \rightarrow \sim 380$-bit field
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Recursion choice

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Post-place-and-route estimation for Xilinx Virtex-II Pro
- $\sim 50000$ slices (2 LUTs 4 $\rightarrow$ 1 per slice)
- 200 MHz
- computes $200 \cdot 10^6$ products per second
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Comparison with parallel-serial multiplier with $D = 16$
- $\sim 8700$ slices
- 180 MHz
- computes $12 \cdot 10^6$ products per second
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<td>2-way Karatsuba with odd-even trick</td>
</tr>
<tr>
<td>5</td>
<td>2-way Karatsuba with odd-even trick</td>
</tr>
<tr>
<td>3</td>
<td>quadratic multiplication</td>
</tr>
</tbody>
</table>

Choose to have 7 pipeline stages

Post-place-and-route estimation for Xilinx Virtex-II Pro
- $\sim 50000$ slices (2 LUTs $\rightarrow 1$ per slice)
- 200 MHz
- computes $200 \cdot 10^6$ products per second
- 4000 products per second and per slice

Comparison with parallel-serial multiplier with $D = 16$
- $\sim 8700$ slices
- 180 MHz
- computes $12 \cdot 10^6$ products per second
- 1400 products per second and per slice
Outline of the talk

▶ Small characteristic finite fields

▶ Multiplication algorithms and hardware implementation

▶ A finite field coprocessor

▶ Finite fields of composite extension degree
Designing a finite field coprocessor

▶ Determine the specific needs of operations of your computation
Designing a finite field coprocessor

- Determine the **specific needs** of operations of your computation

- **Example:** final exponentiation in pairing computation

```
Register file
```

```
Parallel-serial multiplier
D coeffs / cycle
⌈m/D⌉ cycles / product
```

```
double Frobenius (·)^9
feedback loop
```

```
N. Estibals — Hardware implementation of the arithmetic of fields of characteristic 2 and 3
16 / 23
```
Designing a finite field coprocessor

▸ Determine the **specific needs** of operations of your computation

▸ **Example:** final exponentiation in pairing computation
  - Low **silicon footprint** design

![Diagram of Register file and Unified operator with Frobenius (·)^3]

N. Estibals — Hardware implementation of the arithmetic of fields of characteristic 2 and 3
Designing a finite field coprocessor

- Determine the specific needs of operations of your computation

- **Example:** final exponentiation in pairing computation
  - Low silicon footprint design
  - Many multiplications

---

**Register file**

**Unified operator**

| Addition / subtraction | Frobenius (·)³ |

**Parallel–serial multiplier**

| D coeffs / cycle | $\lceil m/D \rceil$ cycles / product |
Designing a finite field coprocessor

- Determine the **specific needs** of operations of your computation

  - **Example**: final exponentiation in pairing computation
    - Low **silicon footprint** design
    - Many multiplications
    - Long **chains of Frobenius** automorphism application

![Diagram showing components and calculations]

- **Register file**
- **Unified operator**
  - addition / subtraction
  - Frobenius $(\cdot)^3$
  - double Frobenius $(\cdot)^9$
  - feedback loop
- **Parallel–serial multiplier**
  - $D$ coeffs / cycle
  - $\lceil m/D \rceil$ cycles / product
Designing a finite field coprocessor

- Determine the **specific needs** of operations of your computation

- **Example**: final exponentiation in pairing computation
  - Low silicon footprint design
  - Many multiplications
  - Long chains of Frobenius automorphism application
  - Only one inversion

---

Register file

Unified operator
- addition / subtraction
- Frobenius ($\cdot^3$)
- double Frobenius ($\cdot^9$)
- feedback loop

Parallel–serial multiplier
- $D$ coeffs / cycle
- $\lceil m/D \rceil$ cycles / product
Detailed architecture of the coprocessor (char. 3)
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Outline of the talk

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Composite extension degree

- Needed field might have a composite extension degree

- Tower field construction:
  - $\mathbb{F}_{p^m \cdot n} = \mathbb{F}_{p^m}[y]/(g(y))$
  - $g$ irreducible polynomial of degree $n$
Composite extension degree

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- Tower field construction:
  - $\mathbb{F}_{p^m \cdot n} = \mathbb{F}_p[y]/(g(y))$
  - $g$ irreducible polynomial of degree $n$

- Reducing the datapath
  - design a coprocessor for $\mathbb{F}_{p^m}$
  - program it to implement arithmetic of $\mathbb{F}_{p^m \cdot n}$
  - reduce area of the design

- Operations
  - same algorithms
  - coefficients are now in $\mathbb{F}_{p^m}$
Some other multiplication algorithms

- Subproducts between field elements, not polynomials
  - no overlapping at reconstruction step

- Apply reduction modulo $g$
  - some subproducts may not be needed after reconstruction step
Some other multiplication algorithms

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- Toom–Cook algorithms
  - evaluate and interpolate at some points
  - $\mathbb{F}_p$ does not provide enough interpolation points
  - hardly usable in this case
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  - evaluate the product modulo some irreducible polynomials
  - reconstruct the result thanks to CRT
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- CRT-based algorithms
  - evaluate the product modulo some irreducible polynomials
  - reconstruct the result thanks to CRT

- Montgomery’s Karatsuba-like formulae
  - ad hoc formulae for degree 4, 5 and 6 polynomials

- Algorithmic search for optimal formulae
  - Work in progress with J. Detrey, R. Barbulescu and P. Zimmermann
Choosing multiplication algorithm

- Evaluate the cost of the different algorithms
  - choice depend on the hardware implementation of $\mathbb{F}_{p^m}$
  - additions not always negligible
Choosing multiplication algorithm

- Evaluate the cost of the different algorithms
  - choice depend on the hardware implementation of $\mathbb{F}_{p^m}$
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Multiplication in $\mathbb{F}_{3^m \cdot 5}$

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>$\times$</th>
<th>$+$</th>
<th>Ratio</th>
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</thead>
<tbody>
<tr>
<td>Schoolbook</td>
<td>25</td>
<td>24</td>
<td>0.96</td>
</tr>
<tr>
<td>One-level Karatsuba (Montgomery’s trick)</td>
<td>21</td>
<td>29</td>
<td>1.38</td>
</tr>
<tr>
<td>Recursive Karatsuba</td>
<td>15</td>
<td>39</td>
<td>2.60</td>
</tr>
<tr>
<td>Recursive Karatsuba (Montgomery’s trick)</td>
<td>14</td>
<td>43</td>
<td>3.07</td>
</tr>
<tr>
<td>Montgomery’s Karatsuba-like</td>
<td>13</td>
<td>54</td>
<td>4.153</td>
</tr>
<tr>
<td>CRT-based</td>
<td>12</td>
<td>53</td>
<td>4.42</td>
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</tbody>
</table>
Choosing multiplication algorithm

Evaluate the cost of the different algorithms

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### Multiplication in $\mathbb{F}_{3^m \cdot 5}$

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### Multiplication in $\mathbb{F}_{2^m \cdot 7}$

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<th>$\times$</th>
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<th>Ratio</th>
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</thead>
<tbody>
<tr>
<td>Schoolbook</td>
<td>49</td>
<td>48</td>
<td>0.98</td>
</tr>
<tr>
<td>One-level Karatsuba (Montgomery’s trick)</td>
<td>40</td>
<td>52</td>
<td>1.30</td>
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<tr>
<td>Recursive Karatsuba</td>
<td>25</td>
<td>51</td>
<td>2.04</td>
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<tr>
<td>Recursive Karatsuba (Montgomery’s trick)</td>
<td>23</td>
<td>76</td>
<td>3.30</td>
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<tr>
<td>Montgomery’s Karatsuba-like</td>
<td>22</td>
<td>84</td>
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<tr>
<td>CRT-based</td>
<td>22</td>
<td>88</td>
<td>4.05</td>
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Conclusion

- Accelerators for *curve-based cryptography* rely on *finite field arithmetic*
Conclusion

▶ Accelerators for curve-based cryptography rely on finite field arithmetic

▶ Many criterion for optimization
  • area: low cost devices
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  • area: low cost devices
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  • area-speed tradeoff: high-throughput application
Conclusion

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- Many criterion for optimization
  - **area**: low cost devices
  - **speed**: if security should not introduce latency
  - **area-speed tradeoff**: high-throughput application

- Multiplication is the critical operation
  - many implementation strategies
Conclusion

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- Many criterion for optimization
  - area: low cost devices
  - speed: if security should not introduce latency
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- Multiplication is the critical operation
  - many implementation strategies

- Need for algorithms/hardware codesign
Thank you for your attention!

Questions?