A 802.11g and UMTS Simultaneous Reception Front-End Architecture using a double IQ structure

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Abstract—In this paper, we address the architecture of multistandard simultaneous reception receivers and we aim to reduce the complexity of the analog front-end. To this end, we propose an architecture using the double orthogonal translation technique in order to multiplex two signals received on different frequency bands. A study case concerning the simultaneous reception of 802.11g and UMTS signals is developed in this paper. Theoretical and simulation results show that this type of multiplexing does not significantly influence the evolution of the signal to noise ratio of the signals.

I. INTRODUCTION

Nowadays the market presents a real interest in the development of telecommunication networks based on radiofrequency systems. Along with the already existing ones, new standards (WiFi, WiMax or the 3G standards) allow the operators to offer new and better services in terms of speed, quality and availability. Consequently, in order to handle this important diversity of telecommunication techniques, there is a growing interest in developing new front-end architectures capable of processing several standards.

For the multistandards research domain, we can distinguish two different categories of front-end receivers: non-simultaneous receivers using switching techniques [1][2][3][4][5] and simultaneous receiving receivers [6]. The state of the art of the multistandard simultaneous reception architectures uses the front-end stack-up technique - each chain being dedicated to the reception of only one standard. Nonetheless, this architecture is characterized by some inconveniences such as the bad complexity-performance trade-off, but also the price and the physical size.

The goal of the architecture proposed in this paper, subject of a patent pending [7], is to answer a multistandard simultaneous reception need generated by the ambient or sensor network domain, while also not being restricted to that alone. In order to answer to this need, we chose to study the simultaneous reception of an 802.11g and an UMTS signal.

The structure assessed in this paper implements a novel and innovating multistandard simultaneous receiving architecture using a single front-end. This architecture uses the double IQ technique [8][9] in order to multiplex the two standards signals by completely overlapping their spectrums at an intermediate frequency. After the second IQ translation, the baseband signals are digitized and then processed by a digital block that separately demultiplexes the baseband components of the two standards. Moreover, the baseband signal has the same bandwidth as the one of the state of the art front-end stack-up structure. A key point of this structure is the orthogonal mismatches of the translation blocks, which can be meanwhile digitally mitigated by an appropriate signal processing [10][11][12].

This paper consists of three parts. Following this introduction, section II describes the double IQ principle, along with the implementation of this technique in a novel multistandard front-end architecture. The last section details the implementation of such a receiver by specifying its functionality and by presenting some significant simulation results. Finally, conclusions of this study are drawn and the follow-up to this work is provided.

II. MULTI-BAND RECEIVER USING A DOUBLE IQ STRUCTURE

A. The double IQ technique

In wireless telecommunications, the integration of IQ baseband translation structures in the receiver chain has become a common procedure. The simple IQ architecture is usually used in the receiver front-end design in order to reduce the bandwidth of baseband signals treated by the ADC (Analog to Digital Converters).

Meanwhile, this IQ structure is also used to eliminate the image frequency default during the translation steps of heterodyne front-end architectures [9][10]. It consists in using the double IQ structure described below. This type of image rejection structure relies on the advantage of orthogonalizing the useful signal and the signal occupying its image frequency band. Even though the spectrums of the two signals are completely overlapped after the first frequency translation, this orthogonalization allows the baseband processing to theoretically eliminate the image frequency component while reconstructing the useful one.

This paper assesses the use of the double IQ structure in order to develop a multi-standard simultaneous reception front-end. In fact, the main idea is to reconstruct the signal from the image band in the baseband domain, the image band becoming a second useful signal. This paper deals with system models and implementation considerations of this new architecture in order to reconstruct the two useful signals.

Fig. 1 describes the double IQ structure. The useful components $s_1(t)$ and $s_2(t)$ of the input $s(t)$ are considered as RF domain signals. Therefore these signals can be modeled by the following:

$$s_1(t) = I_1(t)\cos(2\pi f_1 t) + Q_1(t)\sin(2\pi f_1 t), \quad (1)$$

$$s_2(t) = I_2(t)\cos(2\pi f_2 t) + Q_2(t)\sin(2\pi f_2 t), \quad (2)$$

where $\{I_k(t)+jQ_k(t),\ k=(1;2)\}$ are their baseband complex envelope.

Each IQ translation structure multiplies the input by two 90° shifted sinusoids provided by the frequency synthesizers. The first IQ block uses a local oscillator having a frequency

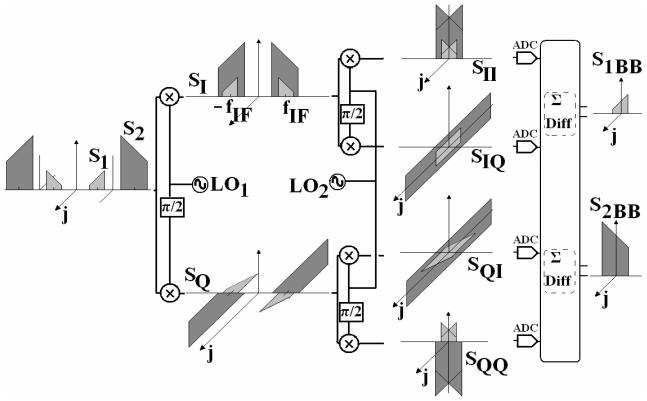

Fig. 1 Spectral evolution of the signals in a double IQ structure

$f_{LO1}=(f_u+f_{Im})/2$. This choice of the oscillator frequency fulfils the image band condition: each of the two signals must occupy the image frequency band of the other before the first orthogonal frequency translation.

By taking into account this oscillator's frequency condition, the two output signals of the first IQ translation structure $s_I(t)$ and $s_Q(t)$ can be defined by:

$$s_I(t) = LP[\cos(2\pi f_{LO1}t)s(t)] = [I_1(t)+I_2(t)]\frac{\cos(2\pi f_{IF}t)}{2} + [Q_1(t)-Q_2(t)]\frac{\sin(2\pi f_{IF}t)}{2} \quad (3)$$

$$s_Q(t) = LP[\sin(2\pi f_{LO1}t)s(t)] = [I_1(t)-I_2(t)]\frac{\sin(2\pi f_{IF}t)}{2} + [Q_1(t)+Q_2(t)]\frac{\cos(2\pi f_{IF}t)}{2} \quad (4)$$

where $LP[.]$ stands for low-pass filter and where the intermediate frequency $f_{IF} = f_1-f_{LO1}=f_{LO1}-f_2$. These equations highlight the overlapping of the useful spectrum and the image band spectrum after the intermediate frequency translation, as shown in *Fig. 1*.

In the second IQ frequency translation step, each of the two signals $s_I(t)$ and $s_Q(t)$ are separately multiplied by two 90° shifted sinusoids. As the frequency of the local oscillators is chosen to be $f_{LO2}=f_{IF}$, the four output signals of this second IQ translation block are translated in the baseband domain and are given by the equations:

$$s_{II}(t) = LP[\cos(2\pi f_{IF}t)s_I(t)] = \frac{I_1(t)}{4} + \frac{I_2(t)}{4}, \quad (5)$$

$$s_{IQ}(t) = LP[\sin(2\pi f_{IF}t)s_I(t)] = \frac{Q_1(t)}{4} - \frac{Q_2(t)}{4}, \quad (6)$$

$$s_{QI}(t) = LP[\cos(2\pi f_{IF}t)s_Q(t)] = \frac{Q_1(t)}{4} + \frac{Q_2(t)}{4}, \quad (7)$$

$$s_{QQ}(t) = LP[\sin(2\pi f_{IF}t)s_Q(t)] = \frac{I_1(t)}{4} - \frac{I_2(t)}{4}. \quad (8)$$

The four output signals contain the multiplexed baseband translated information of the two RF components $s_1(t)$ and $s_2(t)$. The four baseband signals are digitalized and used to perform the demultiplexing step in the digital domain.

This baseband translated information can be separately demultiplexed by two dedicated signal processing, detailed by:

$$s_{1BB}(t) = s_{II}(t) + s_{QQ}(t) + j[s_{QI}(t) - s_{IQ}(t)], \quad (9)$$

$$s_{2BB}(t) = s_{II}(t) - s_{QQ}(t) + j[s_{IQ}(t) + s_{QI}(t)]. \quad (10)$$

Each of these series of operations reconstructs one of the two components while eliminating the other. In fact, by developing (9) and (10) using (5), (6), (7) and (8), we obtain: $\{s_{kBB}(t)=I_k(t)+jQ_k(t),\ k=(1;2)\}$, the same baseband characterizations as those of the RF input signals $s_1(t)$ and $s_2(t)$.

B. Theoretical considerations on the implementation of multi-band double IQ architecture

The complete architecture of the novel multistandard simultaneous reception front-end is shown in *Fig. 2*. The input stages of the front-end are parallelized, each branch being dedicated to the processing of only one frequency band. This way, the signal from the two different frequency bands can be separately received by a dedicated antenna, filtered and amplified by dedicated RF filters and LNA (Low Noise Amplifier) respectively. Another key element of this structure is the power control realized in parallel for the two signals. As it will be shown below this parallel power control step allows a better rejection of the complementary standard during the digital demodulation. Once the signals are properly filtered and amplified, the two signals are processed in order to generate the input signal of the double IQ structure. After the double IQ frequency translation, the four baseband signals are digitized and the two dedicated signal processing reconstruct the two useful signals.

As presented in the previous part, the double IQ structure allows, for ideal orthogonal mismatches conditions, a perfect reconstruction of one signal while cancelling the second. For the receivers using heterodyne process, the image rejection ratio (IRR) is the ratio of the intermediate frequency signal level produced by the desired input signal to that produced by the image band signal. For a double IQ structure, the IRR depends on the gain and phase mismatches between the two branches of the IQ translation structures, and especially on the mismatches of the first one as the frequency translation is generally the highest. The orthogonal mismatches are caused by design and layout defaults such as different line lengths between the two branches and non identical mixers, which generate phase and respectively gain mismatches [12].

For the proposed architecture, the image band rejection is accomplished through a combination between the front-end's input elements: antennas, external RF filters, LNAs on one hand, and the image rejection achieved by the double IQ configuration on the other hand. The state of the art front-end's input elements can realize an image frequency rejection of up to 40 dB depending on the choice of the intermediate frequency.

In order to receive the WLAN 802.11g standard, an IRR of at least 80 dB is needed. In order to achieve this 80 dB IRR, it is shown [11] that only 0.01 dB gain mismatch and 0.1 degrees of phase mismatch are allowed for each of the IQ blocks – this way, the remaining 40 dB of IRR are realized using the image rejection technique.

This high degree of matching is not achievable using only good design and layout techniques, additional digital signal processing techniques have to be employed in order to achieve this performance. One of these techniques has been developed

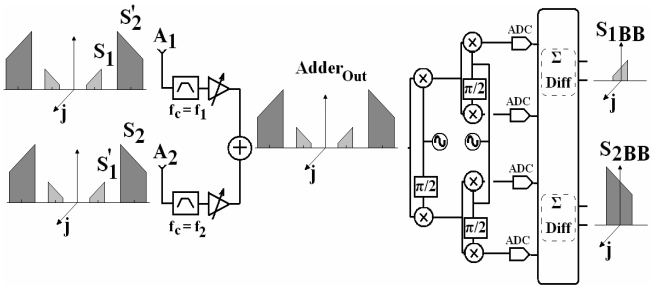

Fig. 2 Multiband simultaneous reception architecture using the double IQ structure

in the digital domain using an LMS (Least mean square) algorithm [11]. The results show an IRR due to the double IQ architecture reaching up to 70 dB.

For the multiband architecture assessed here, the addition of the parallel branches' outputs generates supplementary parasitic signals that can degrade the final SNR (Signal to Noise Ratio) of the two useful signals. Each of the two antennas receives a signal made of two components – $s_1(t)+s'_2(t)$ for the A_1 antenna and $s'_1(t)+s_2(t)$ for the A_2 antenna, where $s_1(t)$ and $s'_1(t)$ are the same transmitted signals after two different propagation channels, as well as $s_2(t)$ and $s'_2(t)$. In fact, for an architecture such as that of *Fig. 2*, the output signal of the adder is mainly composed of four components:

$$Adder_{out}(t) = G_1 \cdot s_1(t) + G_2 \cdot s_2(t) + G'_1 \cdot s'_1(t) + G'_2 \cdot s'_2(t), \quad (12)$$

where the coefficients G_1 , G_2 , G'_1 and G'_2 are the gains that the two input parallel branches of the receiver induce to each of the four components.

In order to evaluate the SNR evolution of the useful signal $s_{1BB}(t)$ after the demultiplexing stage, the evolution of the parasitic signals $s'_1(t)$, $s_2(t)$ and $s'_2(t)$ compared to that of the useful signal $s_1(t)$ have to be taken into account:

- The $s'_2(t)$ signal is attenuated by the input blocks of the branch dedicated to the treatment of $s_1(t)$. These blocks can generate a 40 dB rejection of $s'_2(t)$. The double IQ structure, along with the LMS digital processing, will achieve up to 70 dB of signal rejection from the image band of the useful signal. This means a rejection of up to 110 dB of the parasitic signal $s'_2(t)$.
- The $s_2(t)$ signal undergoes up to 70 dB of rejection compared to the useful signal $s_1(t)$. This rejection is generated by the double IQ structure, similar to that of $s'_2(t)$ as the two signals occupy the same frequency band after the addition of the two branches. In addition to this rejection, another element to be taken into account, when studying the influence of $s_2(t)$ on the SNR of $s_1(t)$, is the dedicated power control stage. In fact the worst case scenario is when $s_1(t)$ is at its lowest power level and the parasitic signal $s_2(t)$ is at its highest. This means that this is the case when $s_2(t)$ has its highest effect on the degradation of the useful signal. In this case, the power control will amplify $s_1(t)$ compared to $s_2(t)$ before the addition step, which means that the influence of the parasitic signal on the useful signal is decreased. The state of the art of the power controls [14] can provide up to 35 dB between minimum and maximum amplification. Therefore, for the worst case scenario, it can be considered that the $s_2(t)$ signal undergoes a 105 dB rejection compared to the useful signal $s_1(t)$.
- The $s'_1(t)$ signal, along with $s_2(t)$, is one of the two components of the radiofrequency signal received by the A_2 antenna. This signal doesn't undergo a rejection due to the double IQ structure as it occupies the same frequency band as the useful signal after the addition step. The only rejection that $s'_1(t)$ will undergo compared to the useful signal $s_1(t)$ is realized by the input elements of the front-end. In fact, as this signal is received by the branch dedicated to $s_2(t)$, the input elements will realize an attenuation of up to 40 dB.

As $s'_1(t)$ and the useful signal $s_1(t)$ are not received by the same antenna, even if they are generated by the same transmitter, a phase shift and a gain shift between the two appears during the RF transmission.

For an AWGN (Additive White Gaussian Noise) transmission channel, the phase shift between the two signals can go from 0 to 360 degrees, but the gain shift can be ignored. For this case, where the two signals $s'_1(t)$ and $s_1(t)$ have the same power level at the input of the front-end, the 40 dB of attenuation of the parasitic signal $s'_1(t)$ achieved before the addition step assures a 40 dB SNR of the useful signal $s_1(t)$ in the baseband domain after the digital signal processing. This SNR level insures a very good reception quality.

In the case of a multipath channel, where the gain shift as well as the phase shift can not be ignored, a new solution can be implemented. It consists in using a digitally controlled RF phase shifter that will cancel the phase shift between $s'_1(t)$ and $s_1(t)$ before the addition step. This way $s'_1(t)$ is no more a parasite, but a useful component during the digital signal processing that reconstructs the $s_1(t)$ signal. This solution will be developed in a future document.

Considering all this arguments concerning the additional parasitic components, it can be considered that the SNR evolution of the useful signal is the same as that of a signal received by a classic mono-standard receiver. Therefore the single front-end multistandard simultaneous reception structure presents similar performance as a front-end stack up structure.

Meanwhile, a complexity comparison study reveals that the single front-end structure is less complex, much more compact and presents a higher on-chip integration level. The number of components is smaller because of the use of a single local oscillator for the first frequency translation compared to the two dedicated oscillators of the front-end stack-up receiver. Furthermore, the greatest advantage of the single front-end receiver is the elimination of the image rejection RF filters. In fact these external components, used to mitigate the impact of the image band signal, can not be integrated on-chip. In the proposed architecture, these components are replaced by a cheaper, on-chip and especially more flexible signal processing. In the following section, a validation of the theoretical result will be presented.

III. IMPLEMENTATION AND PERFORMANCE

In order to validate the theoretical study, a first implementation was simulated using the ADS software provided by Agilent Technologies [13]. The selection of the standards used for this implementation was influenced by their complexity and their deployment as well as by their complementarities in terms of range. These parameters, along with a direct utility of such a structure in the sensor network domain, directed our choice towards the 802.11g and the WCDMA-FDD standards. Regarding this choice, an important point that should be underlined is the implementation constraints imposed by the standards dynamics, but especially by those of the WCDMA-FDD. These dynamics constraints make this standards choice implementation the most delicate.

In order to realize a good performance comparison between the multistandard single frond-end receiver and the front-end stack-up, the blocks used during the simulation have the same typical metrics (gain, noise figure, 1 dB compression point, third order interception point) for both cases. By taking into account all these metrics, a global characterization of the multistandard single front-end receiver is made (*Table 1*).

During this study, it will be considered that the metrics of the blocks used by the two parallel input branches are similar and therefore the performance offered by the front-end for the two standards are identical in terms of noise figure, gain and third order intercept point.

Fig. 3 represents the evolution of the two standards BER (Bit Error Rate) depending on their SNR level at the antenna. This BER evolution was observed using both the multistandard single front-end and the front-end stack-up structures as receivers. The wireless transmission channel was chosen to be AWGN while the translation blocks are considered to be ideal in terms of IQ mismatch. During the simulation of the reception of one of the standards, the antenna power level of the complementary standard is set to the maximum level so that its parasitic influence is the highest.

Under these conditions, the two standards BER evolutions are almost identical for both types of receivers. In fact, using the multistandard single front-end receiver allows the complete rejection of one of the standards during the digital final signal processing as the IQ mismatches are ignored for the moment.

The theoretical study underlines the importance of the IQ mismatches for the performance of a receiver using a double IQ translation. Indeed, it is necessary to realize a good rejection of the image frequency band, which is occupied by the complementary standard. In fact, this rejection relies on two different methods: the gain control realized in the RF domain and the image band rejection realized by the IQ structure. In order to estimate the impact of the orthogonal mismatches on the evolution of the two standards BER, a second set of simulations are realized. The metrics of the receiver used during these simulations are the same as those presented in *Table 1*, except for the gain dynamics of the AGC which take two different values of 35 dB and 40 dB. Concerning the power level of the signals at the antenna, the power level of the concerned standard is at its reference level (the minimum power level that ensures a certain service quality) while the power level of the complementary standard

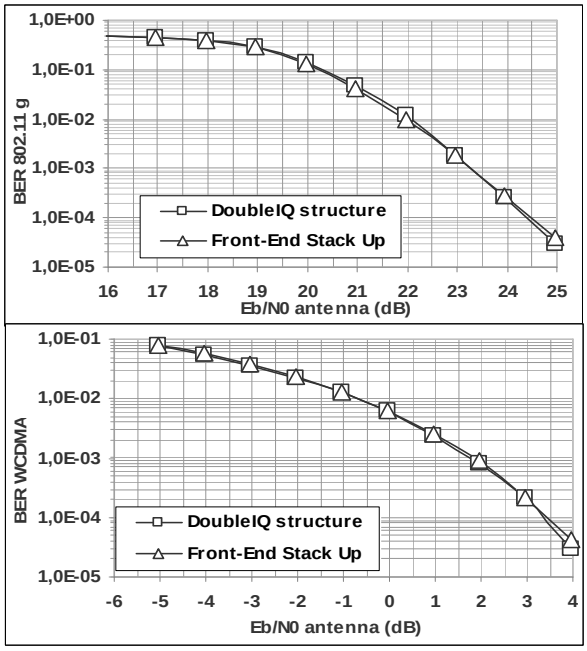

Fig. 3 802.11g and WCDMA BER evolutions during multistandards simultaneous reception using two types of receivers: the classical front-end stack-up and the multistandards single front-end receiver.

TABLE I
METRICS USED FOR THE SIMULATION OF THE MULTISTANDARD SINGLE FRONT-END RECEIVER

Symbol	SI UNIT	VALUE
NF	dB	6
IIP3	dBm	-12
Maximal Gain AGC	dB	25
Minimal Gain AGC	dB	-10

is maximal. For our study case, the concerned standard power level leads to a 10^{-3} level of BER under ideal IQ mismatch conditions.

For each standard, two normalized BER evolutions are presented in *Fig. 4*, for an AGC gain dynamics of 35 and respectively 40 dB. Depending on the AGC dynamics the complementary signal will be attenuated by a certain amount at the input of the antenna compared to the useful signal. Another rejection step is then realized by the IQ structure, but this one is dependent of the orthogonal mismatches.

Results show that the BER performance of the receiver depends on one hand of the AGC gain dynamics and on the other hand on the orthogonal IQ mismatches. For an AGC gain dynamics varying from the state of the art 35 dB to 40 dB, the BER can triple for the same power levels and mismatch configuration. It can also be observed that, under significant orthogonal mismatches conditions, the influence of the complementary standard (at its maximum power level) on the useful one's SNR leads to a BER six times higher.

The results shown in *Fig. 4* do not integrate the digital signal processing (LMS) dedicated to the mitigation of the orthogonal mismatches [11]. The use of these signal processing techniques reduces the final influence of the complementary signal on the useful one's SNR. It can be

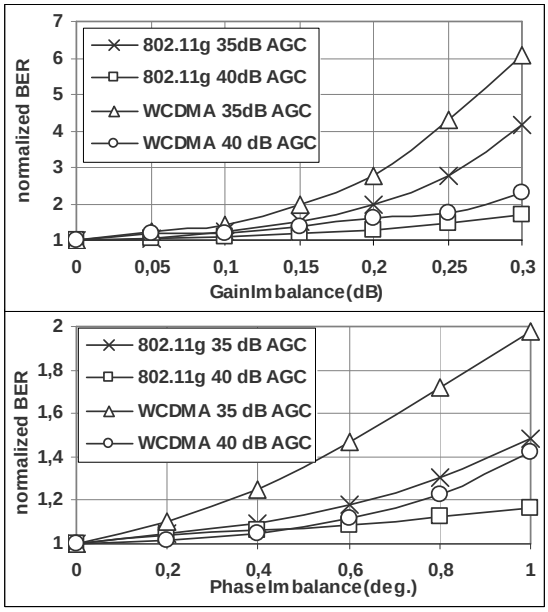

Fig. 4 802.11g and WCDMA BER evolutions versus gain and phase imbalance of the IQ translation blocks. Two series are dedicated to each BER evolution for an AGC gain dynamics of 35 and 40 dB.

considered that the final orthogonal mismatches are reduced to an equivalent level of 0.01 dB of gain mismatch and 0.1 degrees of phase mismatch, corresponding to a 70 dB rejection of the complementary signal from the image frequency band. For these levels of orthogonal mismatches, the influence of the complementary standard on the useful one can be ignored as it can be observed on the results shown in *Fig. 4*. Therefore, the theoretical study concerning the rejection of the parasitic signals presented in section II is validated here.

IV. Conclusions

In this article, a novel multistandard simultaneous reception architecture was presented. Expected performance of its implementation has been presented for a particular study case – simultaneous reception of two signals using the 802.11g and UMTS standards. Compared to the stack-up dedicated front-ends structure, this architecture uses an innovating double IQ multiplexing technique in order to use a unique front-end to receive both standards. In addition to the complexity decrease offered by the use of a single front-end, the signal processed by the analog part of the receiver presets an excellent spectral efficiency as the two standards spectrums are overlapped after the first IQ stage. Knowing that the power consumption of the analog part of the receiver is directly dependent on the bandwidth of the signal, the excellent complexity-power-performance trade-off becomes obvious. The key point of this structure is the rejection of the complementary standard during the demultiplexing stage. As a matter of fact, the rejection level depends of the orthogonal mismatches of the frequency translation blocks; a complete study of their influence has been presented.

The issues that still have to be addressed turn around the implementation of a digital processing used to mitigate the IQ impairments. Another interesting idea concerns a possible multi-antenna multistandard simultaneous reception technique using the principles of the architecture assessed in this article.

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