Design Flow and Run-Time Management for Compressed FPGA Configurations

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Abstract

Partially and dynamically reconfigurable hardware provides an increased flexibility through the load of multiple applications on the same reconfigurable fabric at the same time. However, a configuration bit-stream loaded at runtime should be created offline for each task of the application. Moreover, the use of specialized hardware blocks tends to cancel the single bit-stream for a single application paradigm, as the logic content for different locations of the reconfigurable fabric may be different. We propose a design flow for generating compressed configuration bit-streams abstracted from their final position on the logic fabric. Those configurations are then decoded and finalized in real-time and at runtime by a dedicated reconfiguration controller to be placed at a given physical location. The generated configurations moreover benefit also from a compression factor up to 10×, without using memory-costly algorithms (LZSS) used in the literature [1,2].

Overview of the CAD Flow

The VTR (Verilog To Routing) tool flow [3] is used to synthesize an HDL description up to the placement and routing steps using VPR (Versatile Place-and-Route).

Our custom back-end vbsgen uses the placement data generated by VPR to create a bitstream suitable to the target reconfigurable architecture.

This bitstream is a Virtual Bit-Stream, containing all the routing data in an abstracted representation. This allows to achieve:
- An independence of the VBS from its relative placement on the reconfigurable fabric
- A compression of the bitstream

Virtual Bit-Stream Concept

The repeatable pattern of an FPGA is a Logic Block (LB) surrounded by its interconnection network. Each dot is a 3 or 4-way routing element.

A full bit-stream of this pattern needs to describe the state of each switch!

In sparsely routed areas, the compression gain is huge since little data gets encoded.

Target Architecture

The generated Virtual Bit-Streams are stored in a memory on the target platform and loaded at runtime by a reconfiguration controller.

The complexity of this controller is low since the routing is made on the local interconnection network and has been proved possible offline.

Results

Our results on the 20 biggest MCNC designs shows an average compression ratio of 40%. The most dense designs get the highest ratios.

Clustering multiple basic patterns together leads to compression factors up to 10×, at the cost of more operations needed at run-time.

References